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INTERIM REPORT ON PHASE I EXPANSION OF THE SEISMIC COMMUNICATION AND CONTROL PROCESSOR SYSTEM (CCP)

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INTERIM REPORT ON PHASE I EXPANSION OF THE SEISMIC COMMUNICATION AND CONTROL PROCESSOR SYSTEM (CCP)

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Summary

This is an interim report reviewing the implementation and acceptance testing of the Phase I hardware and software expansion of the Communication and Control Processor (CCP).

The CCP was placed in operation in February 1976 as the central node in a seismic net collecting on-line data from LASA and ALPA over leased lines and from NORSAR over the ARPANET. The system included software for augmenting the ARPANET inputs by adding the planned ILPA, KSRS, and Site II stations.

Plans for the future of the seismic network have been changed and the CCP is being modified to accept on-line data from LASA and four or five North American Network stations over leased lines and from NORSAR over the ARPANET. This represents a potential increase in throughput of about 50%. The CCP is being upgraded in two phases to meet the projected load increase.

The effort described in this report is the first phase of the upgrading. It included increasing the private and shared memory in the CCP, designing and coding the input software for leased line North American Network stations, and a design study for buffered interface hardware for leased line data.

The design study for the buffered line interface was summarized in BBN Report No. 3375.[4] The hardware and software changes to the CCP were completed in December 1976, and acceptance tests were completed in January 1977.

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Introduction

As part of the effort under the VELA program for improving the capability to detect and identify underground nuclear explosions by seismic means, ARPA is supporting the development of a worldwide network of seismic stations. Some of these stations will communicate on-line with the processing center at the Seismic Data Analysis Center (SDAC) and with a large archival storage system at Computer Corporation of America (CCA). The system design makes use of leased lines and the ARPA network for communications in this seismic network. The CCP is the central node in this network; i.e., it accepts data from the seismic stations, reformats the data, and forwards it to the storage and processing facilities.

The CCP was accepted and placed in operation in February 1976, as a part of the SDAC. Since that time, the planned configuration has been modified, and the CCP is being upgraded to meet the projected requirements for the new network configuration in two phases.

This report documents the implementation and testing of the first phase of the upgrading of the CCP.

Additional Memories

Operating experience with the CCP has shown that the delay in the ARPANET communications for the seismic network data is long enough to cause buffer overflow in the CCP with the original planned throughput rate. Since the present planned network configuration may have on the order of a 50% increase in throughput, it was clear that the buffer memory space in the CCP had to be expanded. This memory expansion consisted of adding 4K words to each of the processor private memories, and adding an additional 8K words of shared memory on each M/I bus. The effect of these changes is to add 12K words of buffer memory to each M/I bus and to move more code into private processor memories for more efficient operation.

The CCP is designed to use parity checked memory on the M/I busses, and it was known that parity memory would not operate on a bus extension using a Bus Extender. Since the additional 8K of shared memory would have to go on the bus extension, the changes included replacing the Bus Extender with a Bus Coupler. The additional memory was installed in the CCP in the middle of December 1976. During the acceptance tests, it was found that the parity memory would not operate on the bus extension even using Bus Couplers for the extension. Parity was disabled and the CCP was put in operation using the original Bus Extenders pending further study. No noticable change in system performance has resulted from this modification.

The acceptance tests for these hardware modifications are described in more detail below.

Buffered Synchronous Line Interface Study

In the configuration now planned for the seismic network the input from all seismic stations except NORSAR will be via leased line communication links using 4800 baud synchronous data modems. In the previous configuration only LASA and ALPA used leased lines. Since the Pluribus synchronous line interface was a character-by-character interface, servicing this increased number of synchronous lines would cause unacceptable processor loads and would also put severe strip time restrictions (timing constraints) on all software. The Phase I upgrading, therefore, included a design study to determine the feasibility and cost of replacing the old Synchronous Line Interface (SLI) cards with Buffered Synchronous Line Interface (BLI) cards on a one-for-one basis.

The study concluded that the SLI card could be redesigned to include input and output FIFO queues and optional strapping to reverse signal polarity (to operate with RS-232 or MIL 188C modems) if the existing automatic first SYN character and multiple SYN character deletion logic were removed. Since neither of these SYN character deletion features was being used, the deletion of these features did not present any problem. The detailed analysis of the redesign study is included in BBN Report 3375, The Synchronous Line Interface Study.

Leased Line Input Software Module

In the old network configuration, stations using the format of the KSR site were planned to communicate with the CCP over ARPANET communication links. In the new configuration, stations with this data format will interface with the CCP over leased synchronous lines. The software modification in Phase I of the CCP upgrading consisted of preparing the leased line input software module for receiving data in the KSR format.

The software module was completed in December 1976, and the final tests were run early in January 1977. Since the format from these stations is identical to the VELA output format, testing of the new software module was performed by looping the VELA output back into the CCP as a remote station. A description of the acceptance tests and the resulting test data is given in the next section.

Acceptance Tests

Introduction

The Acceptance Tests for the hardware and software modifications each involved essentially three stages. First, the modification itself was tested. Next the overall system operation and data throughput were demonstrated. Finally, a 25 hour normal operation period was required. Although the test procedures for the hardware and the software modifications were written separately, the actual tests of system operation and the 25 hour run were combined. The hardware acceptance test procedures are included as Appendix A, and the software acceptance test procedures are included as Appendix B.

Hardware Modification Acceptance Tests

Part I of the hardware acceptance tests consisted of demonstrating that the new memories operated correctly and were used by the operational software. The memories were installed and Part I of the tests was performed during the week of November 29, 1976. It was found that the parity checking would not work on the extension of an M/I bus using either Bus Couplers or Bus Extenders. The tests were then performed with parity disabled and the Bus Extenders in use. The tests were successful and the system was left in this configuration.

Part II of the hardware tests consisted of demonstrating the end-to-end data flow, the reliability code, and normal operation of the CCP over a 25 hour period. Since these identical tests had to be performed as part of the software tests, the software and hardware tests were run concurrently at the end of December and the first week in January. These tests are discussed in the next section under acceptance testing of the software modifications.

The responsibility for operation and maintenance of the modified CCP hardware was returned to Geotech starting 12 January of 1977.

Software Modification Acceptance Tests

The acceptance tests for the leased line input software change were performed in three parts. In the first part, the new software module was tested by looping the VELA output back into the CCP and treating it as a leased line input from a KSRS type station. This test was intended to demonstrate the correct operation of the new input module. Due to the fixed time delay required in VELA output data and the consistency checks on time for input data, this test mode will not operate without a software patch to modify the fixed delay on VELA output data. This patch was designed and implemented and an attempt was made to run Part I of the tests with the send side of one modem looped both to its own receive and to another modem receive side to simulate two stations. It was found that the modems would not stay synchronized because the sending modem was trying to train with two different receive modems. When the looping configuration was changed so that a single sender talked to a single receiver, the tests were successful.

The plot from the CCP display at 16:28:11 on January 11, 1977 shows data collected in this looped configuration. The output data that was looped to simulate the two additional sites was the LASA channel displayed. The two simulated stations were KSR and S2Ø.

Part II of the tests was to demonstrate that the new software module did not affect the operation of the rest of the system. The test consisted of repeating parts of the original acceptance tests of the reliability code and of the communication with the DP and SIP to demonstrate the end-to-end data flow through the network.

These tests were logically part of both the hardware and software acceptance test procedures. The reliability software tests were performed on January 7, 1977. The interactive and the output Teletype records from this period are included in the test data volume along with several plots from the CCP display showing test results. The plot at 18:51:12 shows the effect of disconnecting the LASA input. The data gap appears first in the LAO data and nine records later in the looped KSR and S2Ø data. Data reappears when the connector is replaced.

The plot starting at 19:11:53 shows the result of taking power off the "local" processor bus (the bus controlling the operator panel and the display). When power was restored the reliability code was unable to properly restart the processors on that bus. When the same processors were stopped by "halting" the processors using the panel, the system successfully recovered. When power for the "remote" processor bus (not controlling the panel) was turned off and on, the system also recovered. Thus, there is a peculiar state of failure of the "local" processor bus that is not handled correctly in the reliability code and manual

intervention (halting the processors on that bus) is required for full system recovery.

An attempt was then made to split the machine and run the operational program in one half while test programs were running in the other (HALF mode). This test was not completely successful. Although the machine separated into two halves running independently, it was impossible to start the common memory DDT program in this mode, and DDT is essential if the HALF mode is to be useful. A new version of DDT, possibly in local memory, is required to correct this problem. The rest of the reliability tests were conducted successfully.

The end-to-end data flow tests were performed on January 10, 1977. During these tests the data was found to be satisfactory, but status data from the LAO, KSR, and S2Ø site data were not consistent. Since the latter two sites were simulated by using the LAO data, the data status of these three sites should have been identical.

The test data volume includes a plot and listing of data collected in this looped mode taken around the time of 15:08 to 15:42. The data and the plots show that the LAO data is repeated for KSR and S2Ø with the expected 9 second delay. The test data volume also contains a listing of the daily status message for the entire operating part of the network. This message is sent at midnight each day.

In order to explore the status discrepancies an additional test was designed and conducted on January 11. For this test the data from the LAO station was concurrently fed into two independent data collecting systems as shown in the diagram in Figure 1. One path used one of the 360/40 computers to record on tape without using the CCP. The second path used the normal route through the

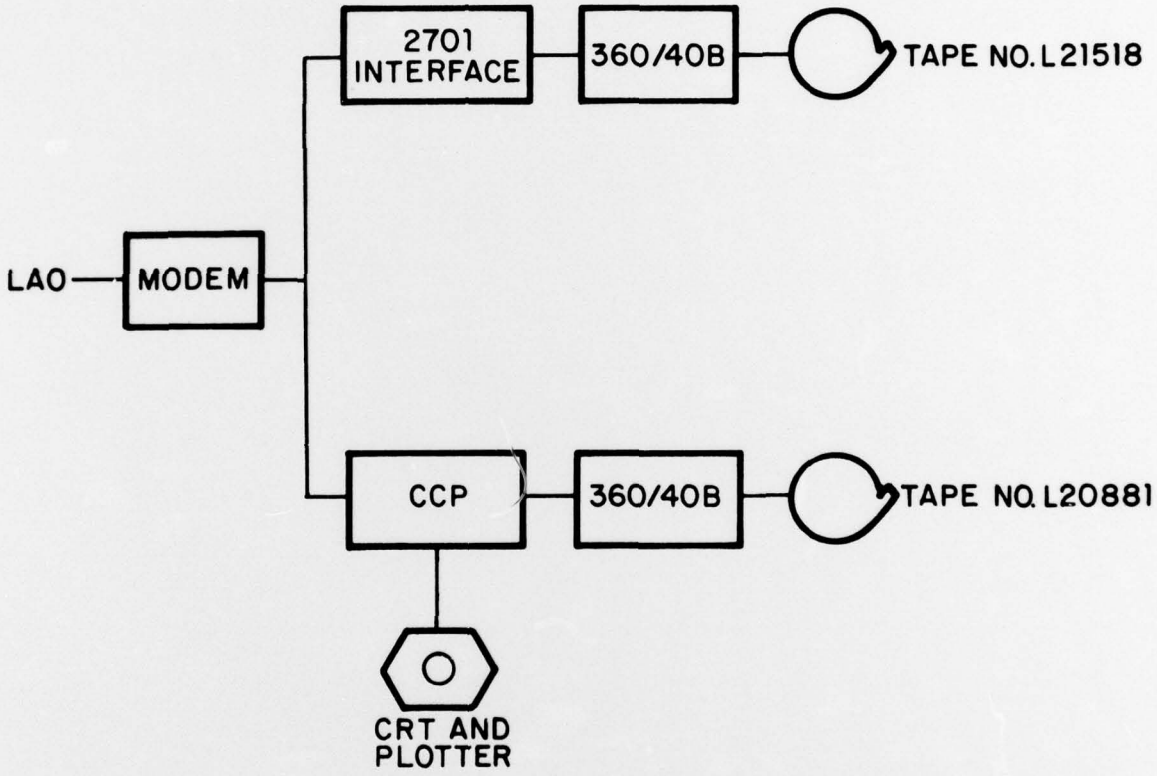

FIGURE 1: Added Test Configuration

CCP to the second 360/40 to record the data. The test data volume contains dumps from each of these tapes. Plots of the data at the CCP and from the tape recorded independent of the CCP are also included for comparison.

After the normal data flow was observed in this test configuration, the LAO input cable to the CCP was disconnected causing the site to appear down, and the status changes associated with this test were observed. The test data volume contains listings of the resulting status messages.

These tests showed that the "data suspect" bits in the simulated sites are being set erroneously, the NORSAR SP repeat indicator is not properly reflected in output to the operator, and the SP status from LAO is being erroneously cleared.

Conclusions

Although the modified CCP is capable of normal operation in its present configuration, several problems requiring further study have been identified in handling status, in reliability code for HALF and processor recovery, and in memory parity. These problems are being analyzed and corrected.

TABLE 1

List of Acronyms

CCP	Communication & Control Processor
BBN	Bolt Beranek and Newman Inc.
SDAC	Seismic Data Analysis Center
CCA	Computer Corporation of America
ARPA	Advanced Research Projects Agency
ALPA	Alaskan Long Period Array
LASA	Large Aperture Seismic Array
NORSAR	Norwegian Seismic Array
SIP	Seismic Input Processor
HIT	System Test Program
DDT	Dynamic Debugging System
SLI	Synchronous Line Interface
BLI	Buffered Synchronous Line Interface
ILPA	Iranian Long Period Array
KSRS	Korean Seismic Research Station
M/I	Memory/Input-Output
FIFO	First-In First-Out
S2Ø	Site II Station Name
KSR	Korean Seismic Research Station Site Name
DP	Detection Processor
LAO	Large Aperture Seismic Array Site Name
SP	Short Period

APPENDIX A

CCP Test Procedures

Leased Line Input Software Modification

CCP Test Procedures
Leased Line Input Software Modification

1. Introduction

In order to test the software modifications made under contract F08606-75-C-0022 P00011 we recommend the following three part test sequence. The first part will demonstrate the new module, a leased line input for KSRS format data. The second part will demonstrate that other software has not been disrupted by the new module. Part 3 will demonstrate overall system operation.

2. Acceptance Test Part 1

The new input module will be tested by looping the VELA II output from the output SLI to a CODEX modem to a second CODEX modem and back into a second SLI. One or more long period signals and one or more short period signals being transmitted over this loop will be displayed on the CCP display before and after the loop. After several minutes of operation the CCP will be halted and corresponding output and input buffers will be dumped for quantitative comparison. Data will also be dumped from the DP and compared to displayed and dumped data from the CCP.

3. Acceptance Test Part 2

3.1 Demonstrate End-to-End Data Flow

Refer to BBN Report 3349. This test procedure consists of repeating the parts of tests 2L and 2M that use LASA, NORSAR, and the leased line input data following detection processor recording procedures used in the original acceptance test and using SIP recording and tests only if convenient.

3.2 Demonstrate Reliability Code

Refer to BBN Report 3349. This test procedure consists of repeating test phase 3 following the original test procedures, but using LASA instead of ALPA as the test leased line input. In addition, a total power failure will be simulated by either shutting off the main power to the CCP or simultaneously shutting off all CCP power distribution units.

4. Acceptance Test Part 3

The system will be run in normal operating conditions with the data loop used in Part 1 for 25 hours. During this test, the CCP will send the equivalent of two KSRS leased line stations to DP.

APPENDIX B

CCP Test Procedures

Added Private and Shared Memory Modification

CCP Test Procedures

Added Private and Shared Memory Modification

1. Introduction

In order to test the hardware modifications made under contract F08606-75-C-0022 P00011, we recommend the following two part test sequence. The first part will demonstrate the new hardware, added private and shared memory. The second part will demonstrate that system operation has not been disrupted by the modification.

2. Acceptance Test - Part 1

The new memory will be tested in three steps. First, the memory test program will be run for 30 minutes. Next, the HIT system test program will be run for two hours. Finally, the operational system will be loaded and started, and the reliability code tables examined to see that the new memory is discovered and used by the operational program.

3. Acceptance Test - Part 2

3.1 Demonstrate End-to-End Data Flow

Refer to BBN Report 3349. This test procedure consists of repeating the parts of tests 2I and 2K that use LASA, NORSAR, and the leased line input data following recording procedures used in the original acceptance test as closely as the present system configuration will allow.

3.2 Demonstrate Reliability Code

Refer to BBN Report 3349. This test procedure consists of repeating test phase 3 following the original test procedures.

3.3 Normal Operation

The system will be run in normal operating conditions for 25 hours.

4. Preliminary Tests

Since BBN is not responsible for equipment maintenance prior to the modification, we request that the tests in Part I of this test procedure by run for the existing system configuration before we take responsibility for the hardware to make the modifications.

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The seismic network and the CCP are being modified to accept on-line data from LASA and four or five North American Network stations over leased lines and from NORSAR over the ARPANET. This represents a potential increase in throughput of about 50%. The CCP is being upgraded in two phases to meet the projected load increase.

The effort described in this report is the first phase of the upgrading.

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It included increasing the private and shared memory in the CCP, designing and coding the input software for leased line North American Network stations, and a design study for buffered interface hardware for leased line data.